**IN THE CLAIMS:**

**Listing of Claims:**

Claims 1-15 (Cancelled)

Claim 16. (Currently Amended) A microprocessor system for executing Virtual Machine bytecodes which have been translated into a sequence of respective 8-bit microprocessor instructions which correspond either to a fixed and predefined operation or to a user defined operation, the system comprising:

a central processing unit;

an instruction memory for storing the sequence of 8-bit microprocessor instructions;

means for fetching each stored instruction in turn and for analyzing each instruction to determine whether [[an]] each instruction corresponds either to a fixed and predefined operation or to a user defined operation;

means for generating an address corresponding to the location of a subroutine if [[an]] a fetched instruction corresponds to a user defined operation,

wherein, in the event that [[an]] a fetched instruction corresponds to a fixed and predefined operation, the fetched instruction is passed to the central processing unit for execution and, in the event that [[an]] a fetched instruction corresponds to a user defined operation, [[a]] the subroutine corresponding to the fetched instruction is called using the generated address.

Claim 17. (Currently Amended) A microprocessor system according to claim 16, wherein instructions corresponding to fixed and predefined operations are distinguished from instructions corresponding to user defined operations by a bit in a predefined bit position of the instruction code, and the means for analyzing each stored instruction is arranged to check for the presence of a ~~bit~~ predefined value in that bit position.

Claim 18. (Currently Amended) A microprocessor system according to claim ~~16~~ 17, wherein ~~the microprocessor system comprises a data memory arranged in use to store code defining said subroutines~~ said distinguishing bit is the most significant bit of the instruction, and the generating means is arranged to shift the instruction to the left by one or more bits.

Claim 19. (Currently Amended) A microprocessor system according to claim ~~17~~ 18, ~~wherein said distinguishing bit is the most significant bit of the instruction code, and the generating means is arranged to shift the code to the left by one or more bits~~ and comprising a program counter register which is arranged to load the bit shifted instruction.

Claim 20. (Currently Amended) A microprocessor system according to claim ~~19~~ 16, ~~and comprising a program counter register which is arranged to load the bit shifted~~

~~instruction~~ wherein the microprocessor system comprises a data memory arranged in use to store code defining said subroutines.

Claim 21. (Currently Amended) A microprocessor system according to claim ~~18~~ 20, wherein the instruction memory is arranged to hold 8-bit wide instructions, while the data memory is arranged to hold 32-bit data values.

Claim 22. (Currently Amended) A microprocessor system according to claim 16, and comprising a hardware stack arranged in use to store a return address when a subroutine is entered, the return address pointing to the next instruction in the instruction memory to be executed when execution of the subroutine is completed.

Claim 23. (Currently Amended) A microprocessor system according to claim 22, wherein the central processing unit, the instruction memory, a data memory, the hardware stack, and a program counter are all coupled to a common bus.

Claim 24. (Currently Amended) A microprocessor system according to claim 23, wherein the central processing unit, the instruction memory, the data memory, the hardware stack, the program counter, and the common bus are integrated onto a single chip.

Claim 25. (Previously Presented) A microprocessor system according to claim 16, wherein the central processing unit contains an arithmetic logic unit and a data stack, and the top two elements of the data stack are connected to the inputs of the arithmetic logic unit and the output of the arithmetic logic unit is connected to an internal data bus.

Claim 26. (Previously Presented) A microprocessor system according to claim 25, wherein the top three elements of the data stack contain special-purpose circuits, which enable the execution of seven primitive stack operations directly in hardware.

Claim 27. (Currently Amended) A microprocessor system according to claim 16, and comprising means for recognizing a ~~fast-return~~ "fast return" instruction ~~folded~~ "folded" with a regular instruction, by utilizing circuitry which decodes the ~~fast-call~~ "fast call" bit in an 8-bit bytecode and another dedicated bit or bits in the 8-bit bytecode.

Claim 28. (Currently Amended) A microprocessor system according to claim 27, wherein said ~~other~~ another dedicated bit is the second most significant bit in the 8-bit bytecode.

Claim 29. (Previously Presented) A microprocessor system according to claim 16, wherein said Virtual Machine bytecodes are Java bytecodes.

Claim 30. (Currently Amended) A microprocessor system~~, consisting of~~ comprising a central processing unit, 8-bit wide instruction memory, 32-bit wide data memory and a hardware stack connected via an internal bus to ~~the~~ a program counter register, together with an instruction decode unit which includes a circuit for detecting the presence of a distinguished bit in ~~the~~ an 8-bit bytecode, together with a circuit for loading the remaining bits of the bytecode shifted left by a number of bits into the microprocessor's program counter register, while at the same time storing the current value of the program counter register on the aforementioned stack.